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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,309	04/08/2004	Nicholas G. Samra	42P18929	9723

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,309	SAMRA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 8 April 2004. These drawings are deemed acceptable for examination.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Buffer virtualization system and method to allow for a large number of allocatable resources within a microprocessing architecture".

Claim Objections

3. Claims 9-14 and 24-29 are objected to because of the following informalities:

As for claim 9, the phrase "checking whether a whether a" as recited in line 4 of the claim should be changed to "checking whether a" for clarity. A similar objection applies to claim 24, line 6.

Claims 10-14 and 25-29 are objected to for further inheriting the deficiencies of claims 9 and 24 respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 4-14 and 18-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 4 recites in part "physical buffer check (PBC) logic to check whether a virtual buffer index is less than or equal to the HBP". This limitation renders the claim nonenabling, as one of ordinary skill in the art would not be able to ascertain how an index can be compared with a pointer to make a determination whether said index is less than or equal to a pointer. More specifically, one of ordinary skill in the art would be unable to understand how to compare an index with simply an address (i.e. pointer) without undue experimentation pursuant to Applicant's description in the specification. Paragraph 0017 of Applicant's original specification describes indexing the lower bits of virtual buffer address into physical buffer entries, however it is unclear if said index includes these bits (i.e. portion of an address), and if so, how a portion of an address can ever be equal to the address (i.e. pointer) itself.

Claims 6, 7, 9, 18, 20, 21, and 24 are rejected based on the same rationale as claim 4.

Claims that depend directly or indirectly on claims 4, 9, 18, and 24 are further rejected for inheriting the deficiencies of these rejected claims.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 9-14 and 24-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "the buffer" in line 8 of the claim. There is insufficient antecedent basis for this limitation in the claim. More specifically, claim 9 sets forth a "last physical buffer" in lines 2-3 of the claim, and "a buffer" in line 6 of the claim. Which of these two buffers are being referenced here?

Claims 10, and 12-14 are rejected for similar reasons (i.e. reciting "the buffer") as described in the rejection of claim 9.

Claims 24, 25, and 27-29 are rejected based on the same rationale as claims 9, 10, and 12-14, *supra*.

Claims that depend directly or indirectly on claims 9 and 24 are further rejected for inheriting the deficiencies of these rejected claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Paladini et al. (US PG Publication 2005/0033934 A1), hereinafter Paladini.

As for claim 1, Paladini teaches an apparatus comprising:

a plurality of physical buffers to be used by operations associated with computer program instructions (Fig. 2, element 207) – paragraph 0032, all lines; and

virtualization logic to map the physical buffers to a plurality of virtual buffers and to prevent two or more operations that share the same physical buffer from interfering with each other when accessing the same physical buffer (the memory manager (Fig. 2, element 204) uses the virtual space monitor and virtual paging system to map the physical slice buffers to respective virtual slice buffers - paragraph 0031, all lines). Note Paladini further teaches preventing two or more operations that share a physical buffer from interfering with each other. For example, memory contained within a physical slice buffer can be accessed via two "operations", namely a read operation, or a write operation. Since both operations cannot occur simultaneously (i.e. memory is not dual-ported), the system prevents the interference of each operation within a particular buffer by performing these serially, rather than concurrently – paragraph 0032, all lines.

Claim 15 is rejected based on the same rationale as claim 1.

7. Claims 9 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Shinozaki (US Patent 6,836,836 B2).

As for claim 9, Shinozaki teaches a method comprising:

initializing a head buffer pointer (HBP) to point to a last physical buffer in a buffer stack (Fig. 3, each page table consists of stack of buffers. Each buffer contains a head pointer, which points to the last buffer in the stack);

checking whether a whether a virtual buffer index is less than or equal to the HBP and allowing an operation access to a buffer within the buffer stack if the virtual buffer index is less than or equal to HBP, otherwise denying the operation access to the buffer (col. 4, lines 49-64 – the pointer is compared with an index. If the index is larger than the pointer, the access operation to the page table memory cannot proceed, and an error is returned. Otherwise (i.e. smaller or equal to the pointer), the access operation can proceed).

Claim 24 is rejected based on the same rationale as claim 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paladini (US PG Publication 2005/0033934 A1) as applied to claim 1 and 15 above, and in further view of Shinozaki (US Patent 6,836,836 B2).

As for claim 2, though Paladini teaches all the limitations of claim 1, he fails to teach setting a head buffer pointer (HBP) to point to a last physical buffer within the plurality of physical buffers.

Shinozaki however teaches a memory protection control device and method which uses virtual addressing to more efficiently allocate and de-allocate memory buffers (col. 1, lines 44-65). More specifically, Shinozaki teaches a plurality of page tables consisting of stack of buffers. Each buffer contains a head pointer, which points to the last buffer in the stack –Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Paladini to further include Shinozaki's memory protection control device into his own advanced memory architecture. By doing so, Paladini would benefit by exploiting the advantages of minimizing the amount of memory required during the virtual addressing assignment process as described by Shinozaki in col. 1, lines 44-65.

Claim 16 is rejected based on the same rationale as claim 2.

9. Claims 10-14 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinozaki (US Patent 6,836,836 B2) as applied to claims 9 and 24 above, and in further view of Filippo et al. (US PG Publication 2004/0255101 A1), hereinafter Filippo.

As for claim 10, though Shinozaki teaches all the limitations of claim 9, he fails to teach de-allocating the buffer after the operation is retired as recited in this claim.

Filippo however teaches a load store unit with replay mechanism comprising a scheduler configured to issue operations, and load store configured to execute the operations issued by the scheduler (paragraph 0008, all lines). More specifically, Filippo teaches de-allocating memory within the store unit once an operation completes (paragraph 0049, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Shinozaki to further include Filippo's load store unit with replay mechanism into his own memory protection control device. By doing so, Shinozaki would benefit by exploiting the use of data speculation, which could further improve system access time by allowing execution of operations to proceed without waiting for dependency checking to complete as taught by Filippo in paragraph 0007, all lines.

As for claim 11, since Shinozaki discloses directing a pointer to the last buffer in his stack, once the buffer is de-allocated, his pointer would inherently be incremented to maintain a link to the buffer stack elements still remaining.

As for claim 12, Shinozaki teaches permitting access upon successfully comparing the pointer value with the index after the pointer is incremented provided the comparison renders a value less than or equal to the index (paragraph 0049, all lines).

As for claims 13 and 14, Filippo teaches a using both store and load buffers to execute store and load operations (paragraph 0009, all lines).

Again, it would have been obvious to one of ordinary skill in the art at the time of the invention for Shinozaki to further include Filippo's load store unit with replay mechanism into his own memory protection control device. By doing so, Shinozaki could benefit by having a means of exploiting the use of data speculation, which could further improve system access time by allowing execution of operations to proceed without waiting for dependency checking to complete as taught by Filippo in paragraph 0007, all lines.

Claims 25-29 are rejected based on the same rationale as claims 10-14.

10. Claims 3-8 and 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Paladini (US PG Publication 2005/0033934 A1) and Shinozaki (US Patent 6,836,836 B2) as applied to claims 2 and 16 above, and in further view of Filippo (US PG Publication 2004/0255101 A1).

As for claim 3, though the combined teachings of Paladini and Shinozaki teach all the limitations of claim 2, they fail to teach logic to increment the HBP if a buffer is de-allocated.

Filippo however teaches a load store unit with replay mechanism comprising a scheduler configured to issue operations, and load store configured to execute the operations issued by the scheduler (paragraph 0008, all lines). More specifically, Filippo teaches de-allocating memory within the store unit once an operation complete (paragraph 0049, all lines).

As for claim 4, Shinozaki teaches physical buffer check (PBC) logic to check whether a virtual buffer index is less than or equal to the HBP (col. 4, lines 49-64 – the

pointer is compared with an index. If the index is larger, the access operation to the page table memory cannot proceed, and an error is returned. Otherwise (i.e. smaller or equal to the pointer) the access operation can proceed.

As for claim 5, Filippo teaches the PBC logic is within a scheduler unit within a microprocessor (paragraph 0008, all lines).

As for claim 6, Filippo teaches unconditionally storing the operations in the scheduler unit (paragraph 0008, all lines).

As for claim 7, Paladini teaches allocating buffer operation only if the virtual buffer index is less than or equal to the HBP (col. 4, lines 49-64).

As for claim 8, Filippo teaches a load operation (paragraph 0009, all lines), and Shinozaki teaches the virtual buffer index is a virtual load/store buffer index (col. 3, lines 49-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Paladini to further include Filippo's load store with replay mechanism into his own advanced memory management architecture. By doing so, Paladini could benefit by having a means of exploiting the use of data speculation, which could further improve system access time by allowing execution of operations to proceed without waiting for dependency checking to complete as taught by Filippo in paragraph 0007, all lines.

Claims 17-23 are rejected based on the same rationale as claims 3-8.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Perry (US Patent 6,067,608) teaches a high performance mechanism for managing allocation of virtual memory buffer to virtual processes on a least recently used basis.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

9/29/06
MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER